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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,048	04/08/2004	Sadanand V. Deshpande	FIS920030397US1	3047

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EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
12/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,048	DESHPANDE ET AL.	
	Examiner	Art Unit	
	JOHN C. INGHAM	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,9,12-14,27 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,9,12-14,27 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission (Amendments to Claims and Specification) filed on 15 September 2008 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1, 2 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Luning and Fulford.

4. Regarding claims **1 and 14**, Luning discloses in Fig 6 a complementary metal oxide semiconductor (CMOS) device structure comprising: an NFET gate conductor (41) and a PFET gate conductor (42) formed on a substrate (40); first spacers (60, of silicon nitride col 2 ln 57) formed on sidewalls of said NFET gate conductor and said PFET gate conductor; first impurity source/drain implant regions 61) formed in said substrate, substantially adjacent to outer edges of said first spacers (61 is aligned to

spacers 60, and separated from the gate electrode 41 by distance W_2) formed on said sidewalls of said NFET gate conductor; second spacers (of silicon nitride col 2 ln 57) formed on outer sidewalls of said first spacers, first spacers being formed on said sidewalls of said PFET gate conductor (spacer 60 is formed on spacer 44 of gate 42); and second impurity source/drain implant regions, formed in said substrate, substantially adjacent to outer edges of said second spacers (62 is aligned to spacers 60, and separated from the gate electrode 42 by distance W_3) formed on said outer sidewalls of said first spacers formed on said sidewalls of said PFET gate conductor.

5. Luning does not specify an etch stop layer interposed between inner sidewalls of said second nitride spacers and said outer sidewalls of said first nitride spacers. Instead Luning recites merely that removal of the nitride sidewall spacers is effected by etching (col 4 ln 5-7).

6. Fulford teaches in Fig 12 that an oxide etch stop layer (150) is interposed between a nitride spacer (138) and another nitride layer (158) to act as an etch stop so that a second set of nitride spacers can be formed (col 9 ln 4-12). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Fulford in order to form a second set of nitride spacers.

7. Regarding claim **2**, Fulford teaches in Fig 12 that an oxide liner is formed directly on tops and sidewalls of transistor gate conductors and also directly on areas of said substrate not covered by said gate conductors, to act as an etch stop so that the subsequent spacers can be formed and removed separately (col 8 ln 17-22).

8. Claims **7 and 27** are rejected 35 U.S.C. 103(a) as being unpatentable over Luning, Fulford and Gardner (US 5,882,973).

9. Luning and Fulford disclose the CMOS device structure of claim 2, but do not specify silicide regions formed on exposed areas of said oxide layer over said substrate and tops of said NFET gate conductor and said PFET gate conductor. Instead, Luning teaches a cobalt silicide formed directly on exposed areas of the substrate and gate conductors.

10. Gardner teaches in Fig 6 and Fig 7 that exposed areas of an oxide layer over a substrate and tops of gate conductors are silicided with a two step process in order to enhance conductivity (col 8 ln 20). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Gardner on the device of Luning and Fulford in order to enhance conductivity. Luning discloses the cobalt silicide of claim 27.

11. Claims **9 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Luning, Fulford and Wu (US 6,730,556).

12. Luning and Fulford do not specify wherein a first impurity of said first impurity source/drain implant regions comprises arsenic, or wherein a second impurity of said second impurity source/drain implant regions comprises boron. Instead Luning discloses that the first impurity is n-type and the that the second impurity is p-type.

13. Wu teaches that a suitable n-type dopant for CMOS transistors is arsenic, and a suitable p-type dopant for transistors is boron (col 1 ln 64 – col 2 ln 2). It would have

been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Wu since one of ordinary skill in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination yielding no more than predictable results.

14. Claims **13 and 37** are rejected under 35 U.S.C. 103(a) as being unpatentable over Luning, Fulford and Figura (US 5,750,441).

15. Luning and Fulford disclose the CMOS device structure of claim 1, but do not specify wherein said etch stop layer comprises a low temperature oxide.

16. Figura teaches that an etch stop layer preferably comprises a low temperature oxide so that the formation temperature is low enough to not disturb the previously formed layers (col 2 ln 57). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Figura on the device of Luning and Fulford so as to not disturb the previously formed layer.

Response to Arguments

17. Applicant's arguments filed 15 September 2008 have been fully considered but they are not persuasive. Regarding the argument that Fulford does not recite layer 150 as an etch stop layer between sidewall spacers, Fulford teaches that oxide layers act as an etch stop so that a second set of nitride spacers can be formed (col 9 ln 4-12, nitride/oxide/nitride layers where adjacent layers have dissimilar etch characteristics so that they can be selectively etched).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
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John C Ingham
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Examiner, Art Unit 2814